IN THE CLAIMS

Please amend claims 1, 4, 5, 13, 16, 17, and 27 as follows:

Claims 1, 4, 5, 13, 16, 17, and 27 have been amended as follows:

1. (Amended) A computer-implementable method of performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, said method comprising:

non-iteratively processing N mod D to produce the remainder R, where $D=2^n-1$ and $0<N<(D-1)^2$.

~~4.~~ (Amended) The computer-implementable method of claim ~~37~~ 5, further comprising the step of subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

~~5.~~ (Amended) The computer-implementable method of claim ~~38~~ 11, further comprising the step of subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

~~16.~~ (Amended) The apparatus of claim ~~41~~ 23, said apparatus subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

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17. (Amended) The apparatus of claim 42, said apparatus subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

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27. (Amended) The apparatus of claim 13, wherein said apparatus is a component of a Reed-Solomon coder.

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Please add the following claims:

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36. (New) The computer-implementable process of claim 1, further comprising the step of using said remainder R to perform Reed-Solomon coding of data on a computer.

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37. (New) The computer-implementable method of claim 1, further the step of summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lceil \frac{n}{2} \rceil$ bits of the dividend N to produce the remainder R.

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38. (New) The computer-implementable process of claim 2, further comprising the step of using said remainder R to perform Reed-Solomon coding of data on a computer.

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39. (New) The computer-implementable method of claim 2, further the step of summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lceil \frac{n}{2} \rceil$ bits of the dividend N to produce the remainder R.

40. (New) The computer-implementable process of claim 3, further comprising the step of using said remainder R to perform Reed-Solomon coding of data on a computer.

41. (New) The apparatus of claim 13, further the step of summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lceil \frac{n}{2} \rceil$ bits of the dividend N to produce the remainder R.

42. (New) The apparatus of claim 14, further the step of summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lceil \frac{n}{2} \rceil$ bits of the dividend N to produce the remainder R.

43. (New) The apparatus of claim 27, wherein said Reed-Solomon coder performs coding in data communication operations.

44. (New) The apparatus of claim 25, wherein said Reed-Solomon coder performs coding in data communication operations.

45. (New) The apparatus of claim 26, wherein said Reed-Solomon coder performs coding in data communication operations.

46. (New) The apparatus of claim 32, said computer signal being executed on a computer to perform Reed-Solomon coding of data.--